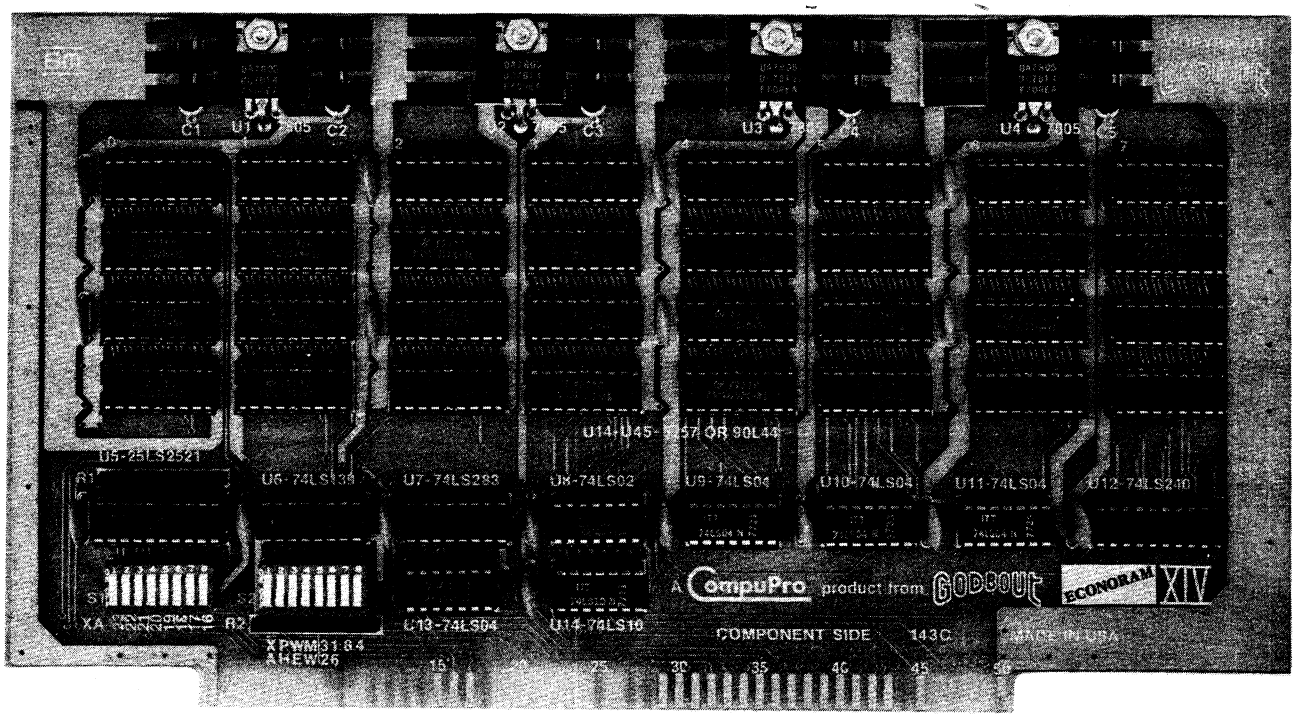
ECONORAM XIV™
USER'S MANUAL



IEEE · S-100
16K Memory 24 Bit Address
using MM5257/90L44 • 5MHz

143
mac

CompuPro™ from GODBOUT

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Table of contents

ABOUT ECONORAM XIV

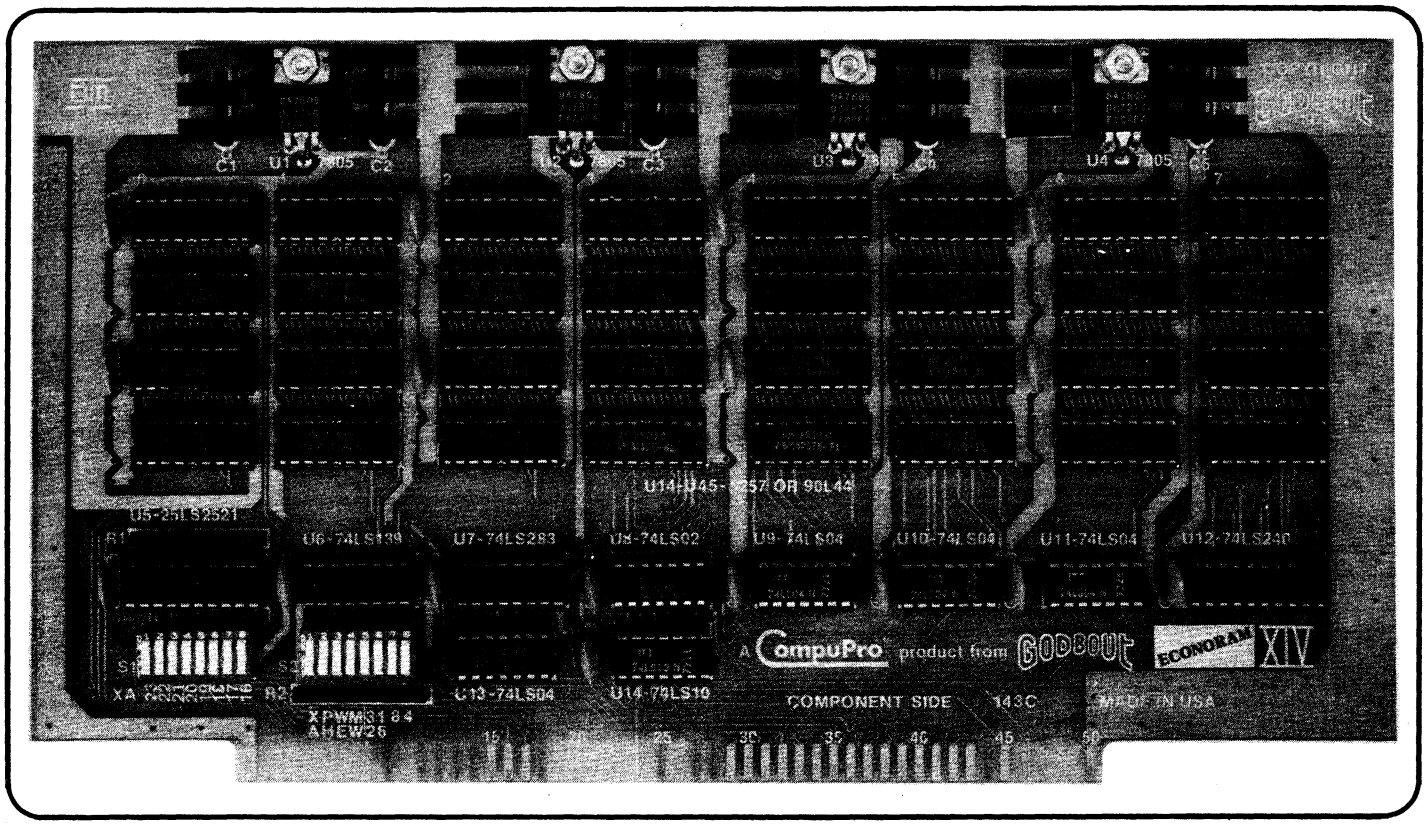
Congratulations on your decision to purchase **ECONORAM XIV**, a 16K x 8 memory board designed specifically for electrical and mechanical compatibility with the IEEE S-100 buss standard. The S-100 buss is the professional level choice for commercial, industrial, and scientific applications. This buss provides for ready expansion and modification as the state of the computing art improves. We believe this board, with the rest of the S-100 portion of the **CompuPro** family, is one of the best boards available for that buss.

As amateur radio operators have contributed greatly to communication technology, so too the computer hobbyist has provided the microcomputer industry with many significant developements. In recognition of this fact, we also make this professional quality board available in "**UNKIT**" form for those who enjoy the challange of assembling and testing a fine computer board.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing a **CompuPro Product** ...welcome to the club!

TECHNICAL OVERVIEW

This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this: static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered...there is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement. The individual memory ICs used on this board are grouped together to form a single 16K x 8 block of memory, addressable on any 4K boundary using the on-board dip switch (no jumpers required). Additional features include a write protect switch; a write strobe selection switch which allows use of this memory in systems with or without a front panel (MWRITE strobe); allowance for use of the PHANTOM* line; extended 24 bit addressing; thorough capacitor bypassing of supply lines to suppress transients; plus on-board regulation and heatsinking for reliably cool operation. All this and sockets for all ICs go onto a double sided, solder-masked printed circuit board with a complete component-layout legend.



BOARD ADDRESSING

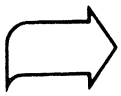
This board is configured as one 16K block. This block may be assigned to any area of memory beginning on a 4K boundary (0K, 4K, 36K etc.) with the only limitation being that it should not overlap any other memory in the system. The board is addressed by flipping S2 positions 5-8 ON or OFF to achieve the desired starting address. With all four switches OFF (S2(5-8)), the block will start at 0H or 0K. To start at 4K, flip switch S2-8 (marked "4" on the legend) ON. To start at 16K or 32K, flip switches S2-6 or S2-7 ON respectively (marked "16" and "32" respectively). To start at 44K, (32K + 8K + 4K) flip switches 32, 8 and 4 ON. In effect, add the switch numbers to give your starting address. Note: If the start of the 16K block is at 52K or above, the residual memory beyond 64K will appear starting at 0K.

EXTENDED ADDRESSING

The ECONORAM XIV has provisions on board for implementing the proposed IEEE S-100 extended address lines, A16-A23. If provided with this option, switch S2 position 1 should be turned OFF to enable the extended address decoder. Switch S1 should be set as shown below.

SWITCH POSITION	FUNCTION	
1	Address A23	
2	Address A22	
3	Address A21	ON = "0"
4	Address A20	
5	Address A19	
6	Address A18	OFF = "1"
7	Address A17	
8	Address A16	

EXAMPLE: To address your Econoram XIV at 370000H, flip positions 3, 4, 6, 7, & 8 OFF and 1, 2, & 5 ON.



NOTE: If not using the extended addressing feature of this board, remove U5 (25LS2521), turn all positions of S1 OFF and turn S2-1 ON.

MEMORY PROTECT SWITCH

If you desire to "write protect" the contents of your **ECONORAM XIV** board; simply turn OFF switch WE (S2-3). With this switch OFF, the content of the RAM can be read, but not altered. For operation as a standard RAM board, leave switch S2-3 ON.

WRITE STROBE SELECTION

Switch S2 position 4 and jumper J1 allow the **ECONORAM XIV** to be operated in several different modes concerning the signal MWRITE (Pin 68). For systems that have MWRITE implemented, turn Switch MW (S2-4) ON. In systems where MWRITE is grounded, turn MW ON (S2-4), for systems that have a floating MWRITE line, turn MW ON and install a jumper at position J1 (in between U13 and U14).

PHANTOM LINE

Switch S2 position 2 allows the **ECONORAM XIV** to be removed from memory space by a low level on PHANTOM* (Bus Pin 67). With S2-2 ON, memory will disappear when PHANTOM* is asserted. With S2-2 OFF, the board is unaffected by PHANTOM*. NOTE: Since some manufacturers are not conforming to the proposed IEEE S-100 buss standard, insure that your system is using the PHANTOM* line properly before using this feature on your **ECONORAM XIV**.

MEMORY TESTING

If the memory board seems to be working properly, the MEMORY TESTING ROUTINE can be used to give the board a more thorough workout. It is rather slow; but will do the job well. It can be entered via editor/assembler or front panel switches.

The routine is set up to test 16K from 4000 hex to 7FFF hex. This may be changed by entering a different starting address at "STRT" (3001-3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical informaton is stored and the routine enters a software "HALT" that is a "jump to here" at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure information:

3069*	"FDE"	= D,E pair...D is the fill character, and E is the test character
306B*	"FHL"	= H,L pair...the failure address
306D*	"FOUT"	= the data expected
306E*	"FIN"	= the data read

* address from MEMORY TESTING ROUTINE

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference betwen "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

MEMORY TESTING ROUTINE

```
3000 21 00 40          0010 STRT LXI  H,40C0H
3003 3E 80             0020 END  MVI  A,80H
3005 32 6E 30          0030      STA  FIN
3008 3E 10             0040      MVI  A,10H
300A 84                0050      ADD  H
300B 4F                0060      MOV  C,A
300C 16 00             0070      MVI  D,0
300E 1E FF             0080      MVI  E,0FFH
3010 22 65 30          0090 DONE SHLD STAD
3013 AF                0100      XRA  A
3014 47                0110      MOV  B,A
3015 7B                0120 SCND MOV  A,E
3016 5A                0130      MOV  E,D
3017 57                0140      MOV  D,A
3018 79                0150      MOV  A,C
3019 2A 65 30          0160      LHLD STAD
301C 72                0170 FILL MOV  M,D
301D 23                0180      INX  H
301E BC                0190      CMP  H
301F C2 1C 30          0200      JNZ  FILL
3022 2A 65 30          0210      LHLD STAD
3025 73                0220 NEXT MOV  M,E
3026 7B                0230      MOV  A,E
3027 BE                0240      CMP  M
3028 C2 6F 30          0250      JNZ  FAIL
302B 79                0260      MOV  A,C
302C 23                0270      INX  H
302D 94                0280      SUB  H
302E C2 4D 30          0290      JNZ  NDON
3031 B8                0300      CMP  B
3032 44                0310      MOV  B,H
3033 CA 15 30          0320      JZ   SCND
3036 3A 66 30          0325      LDA  STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA  FIN
303F B9                0350      CMP  C
3040 CA 00 30          0360      JZ   STRT
3043 79                0370      MOV  A,C
3044 67                0380      MOV  H,A
3045 2E 00             0390      MVI  L,0
3047 C6 10             0400      ADI  10H
3049 4F                0410      MOV  C,A
304A C3 10 30          0420      JMP  DONE
304D 22 67 30          0430 NDON SHLD NXAD
3050 7A                0440 LOPB MOV  A,D
3051 BE                0450 LOPA CMP  M
3052 C2 6F 30          0460      JNZ  FAIL
3055 2C                0470      INR  L
3056 C2 51 30          0480      JNZ  LOPA
3059 79                0490      MOV  A,C
305A 24                0500      INR  H
305B BC                0510      CMP  H
305C C2 50 30          0520      JNZ  LOPB
305F 2A 67 30          0530      LHLD NXAD
3062 C3 25 30          0540      JMP  NEXT
3065                   0550 STAD DS   2
3067                   0560 NXAD DS   2
3069                   0570 FDE  DS   2
306B                   0580 FHL  DS   2
306D                   0590 FOUT DS   1
306E                   0600 FIN  DS   1
306F 22 6B 30          0610 FAIL SHLD FHL
3072 32 6D 30          0620      STA  FOUT
3075 7E                0630      MOV  A,M
3076 32 6E 30          0640      STA  FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD FDE
307D C3 7D 30          0670 SHLT JMP SHLT
3080                   0680 *
```

User Notes:

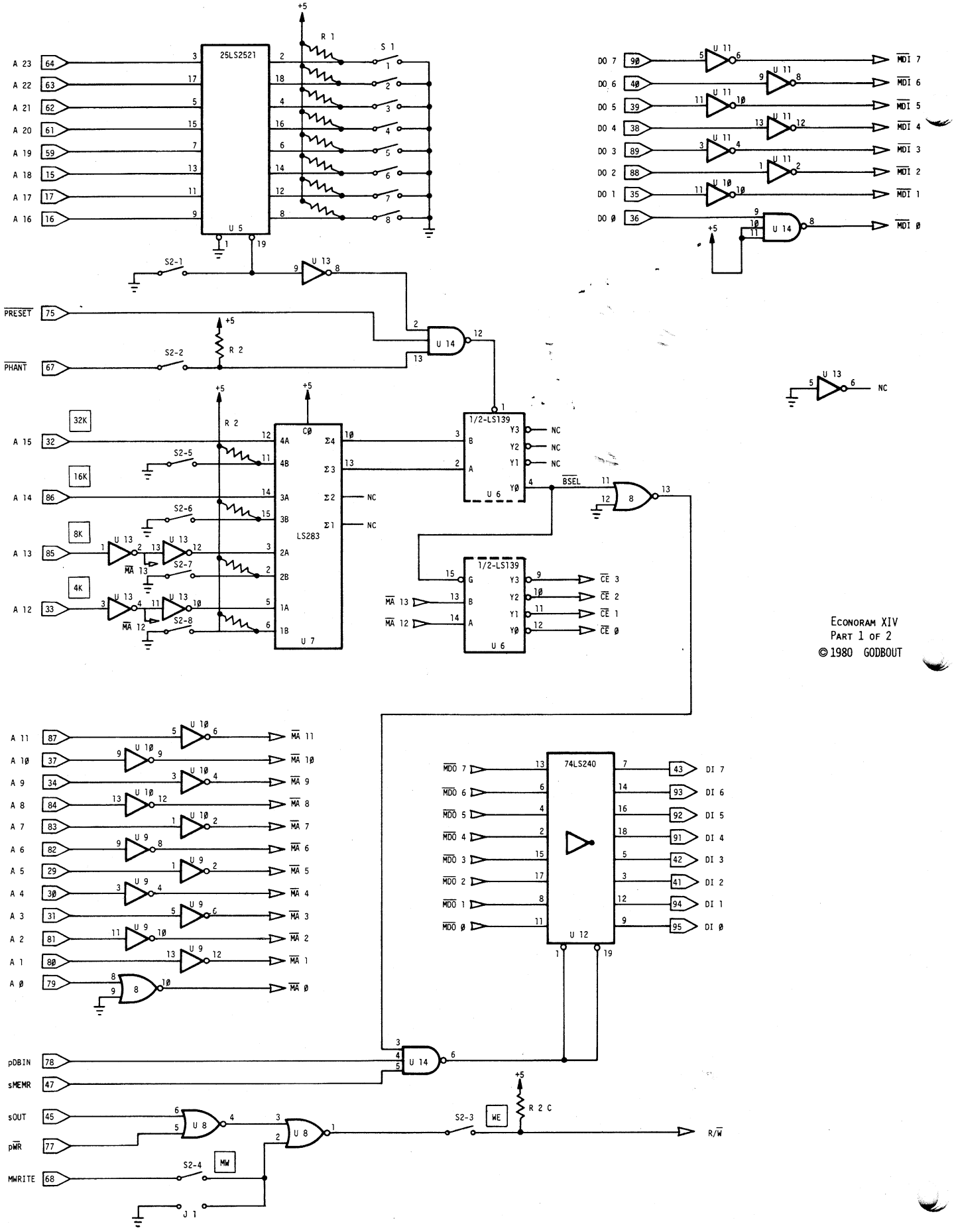
CIRCUIT DESCRIPTION

The heart of **ECONORAM XIV** is the MM5257/90L44 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts. These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4K x 8 bits of information. Paralleling 4 of these rows together produces a total memory storage of 16K x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array). Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to write data into the memory, or read data from the memory. The schematics show the address circuitry along with the other **ECONORAM XIV** circuitry. Each memory IC requires 12 address lines (A0-A11) to access any one of the 4096 bits available in the IC. These address lines are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to react to the given address. This requires 4 more address lines (A12-A15) which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array). When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss). Data to be read to the data buss from memory passes through 8 TRI-STATE inverting buss drivers; when data is not being read to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state.

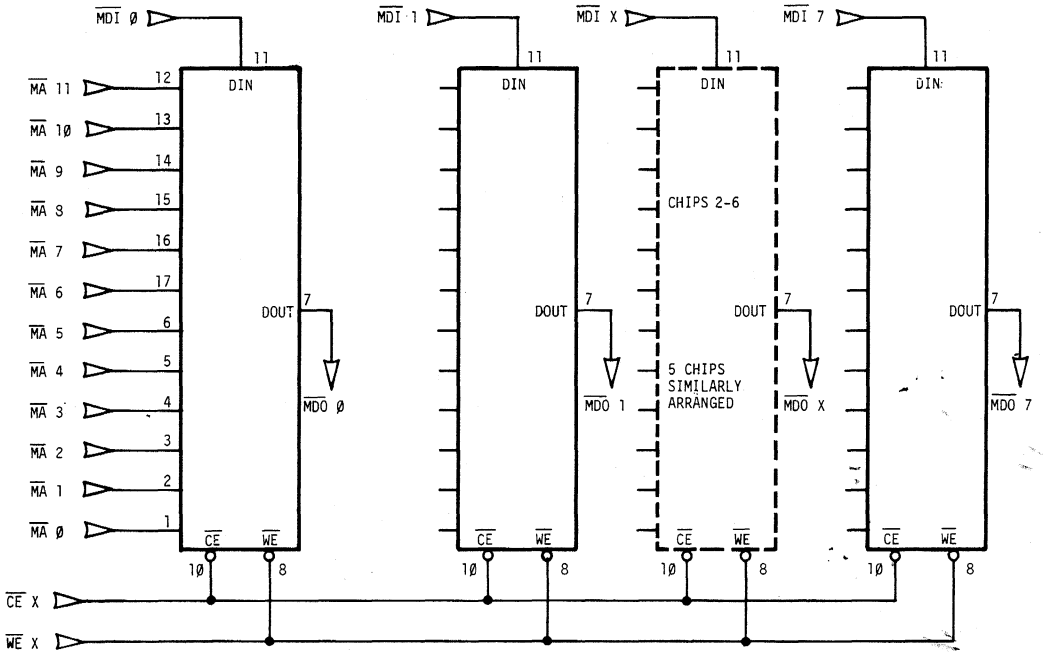
An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC.

This board is guaranteed to operate at 4 MHz, or 5 MHz with an 8085 CPU over the full temperature range (0-70 C ambient) and draw less than 2.0 Amps. Also, our typical measured currents were less than 1.6 Amps, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

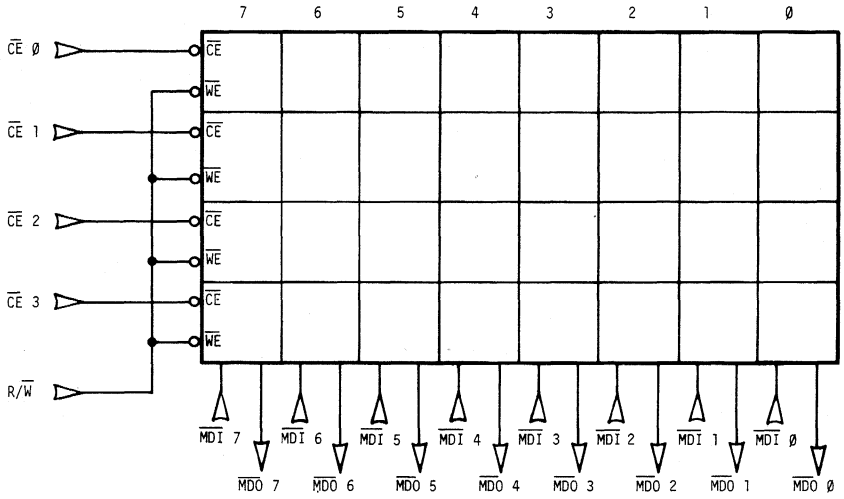
It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

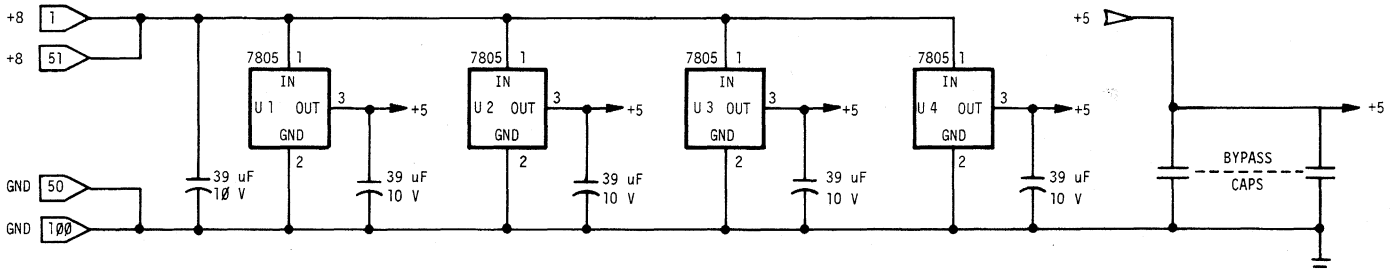


ECONORAM XIV
PART 1 OF 2



ECONORAM XIV
PART 2 OF 2





Parts List

☐ (1) Econoram XIV circuit board.

INTEGRATED CIRCUITS (note: the following parts may have letter suffixes and prefixes along with the key numbers given below.)

☐	(32)	MM5257-3L	4Kx1 static RAM	(U14-U45)
☐	(1)	74LS02	Quad 2 input NOR gate	(U8)
☐	(4)	74LS04	Hex inverters	(U9,10,11,13)
☐	(1)	74LS10	Triple 3 input NAND gate	(U14)
☐	(1)	74LS240	Octal TRI-STATE inverters	(U12)
☐	(1)	74LS283	4 bit adder	(U7)
☐	(1)	74LS139	Dual 1 of 4 decoder	(U6)
☐	(4)	7805	Positive 5V regulators	(U1-U4)

OTHER ELECTRONIC COMPONENTS

☐	(5)	39uF tantalum capacitors	(C1-C6)
☐	(16)	Ceramic disk bypass capacitors *	
☐	(1)	2.7K SIP *	

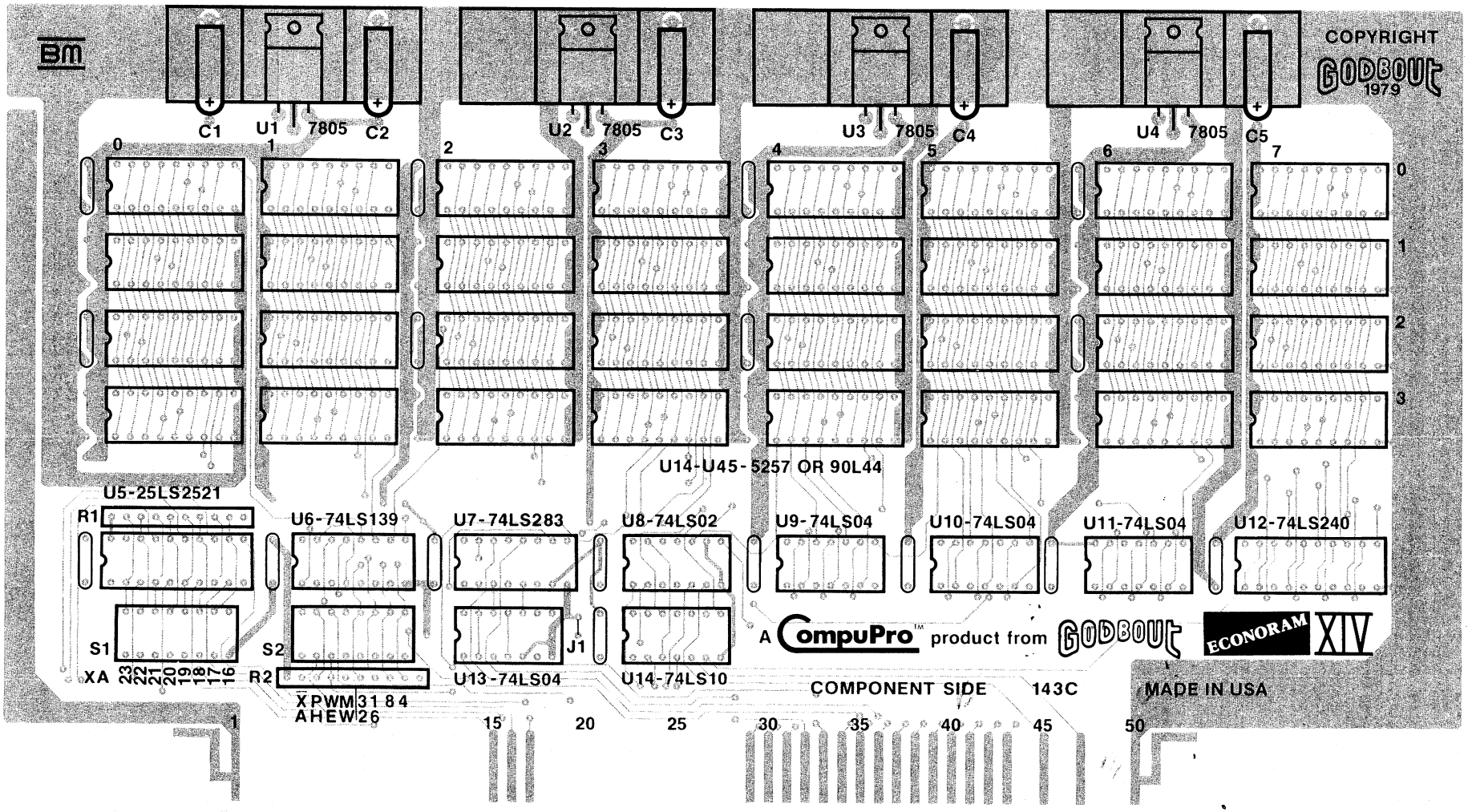
MECHANICAL COMPONENTS

☐	(41)	Low profile sockets *	
☐	(1)	8 pole dip switch	(S1)
☐	(4)	Heat sinks for regulator ICs	
☐	(4)	6-32 bolts	
☐	(4)	6-32 lockwashers	
☐	(4)	6-32 nuts	
☐	(1)	Instruction booklet	

*Supplied already soldered to board

OPTIONAL PARTS FOR EXTENDED ADDRESSING

☐	(1)	25LS2521 Octal Comparator	(U5)
☐	(1)	DIP switch	(S1)
☐	(1)	2.7K SIP	(R1)
☐	(1)	Disc Cap	



Component Layout

CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuPro product. If this product fails to operate properly, it may be returned to us for service; see warranty information below.

If you need further information feel free to write us at:

P.O. Box 2355, Oakland Airport, CA 94614.

When writing, please be as specific as possible concerning the nature of your query. We maintain a 24 hour a day phone for taking orders, (415) 562-0636. If you have any problems or questions which cannot be handled by mail, this number can be used to connect you with our technical people ONLY during normal business hours (10am-5pm Pacific Time). We cannot return calls or accept collect calls.

LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *MUST* be returned for replacement.

If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $10.00.

We are not responsible for damage caused by the use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

Prices and specifications are subject to change without notice, owing to the volatile nature and pricing structure of the electronics industry.